Hardware Monitor for Desktop PCs

Features

Monitoring of All Desktop PC Supplies in Parallel
Internal Comparator Hysteresis
Power Supply Glitch Immunity
Supports Klamath CPU Core Supply Voltage Options
Two-Wire I^2C Compatible Serial Interface
VCC from 2.5V to 6V
Guaranteed Operation from -40C to +85C
No External Components
16 Pin Narrow (150mil) SOIC Package

General Description

The ADM9268 Hardware Monitor IC is a self contained IC which monitors six Power Supplies in a Desktop PC in parallel and outputs the status information on an Industry Standard two-wire I^2C compatible serial interface. There are also two active low event input pins, $\overline{TMP1}$ and TMP2, which might come from temperature sensor circuits, which are added to the status information which can be read through the two-wire serial interface.

Each power supply monitor circuit uses a proprietary window comparator design whereby a three resistor network is used in conjunction with two comparators and a single precision voltage reference to check if the supply is within it's required operating tolerance. An added feature of this design is that the power supply voltages being monitored can be higher than the power supply voltage to the ADM9268 IC itself.

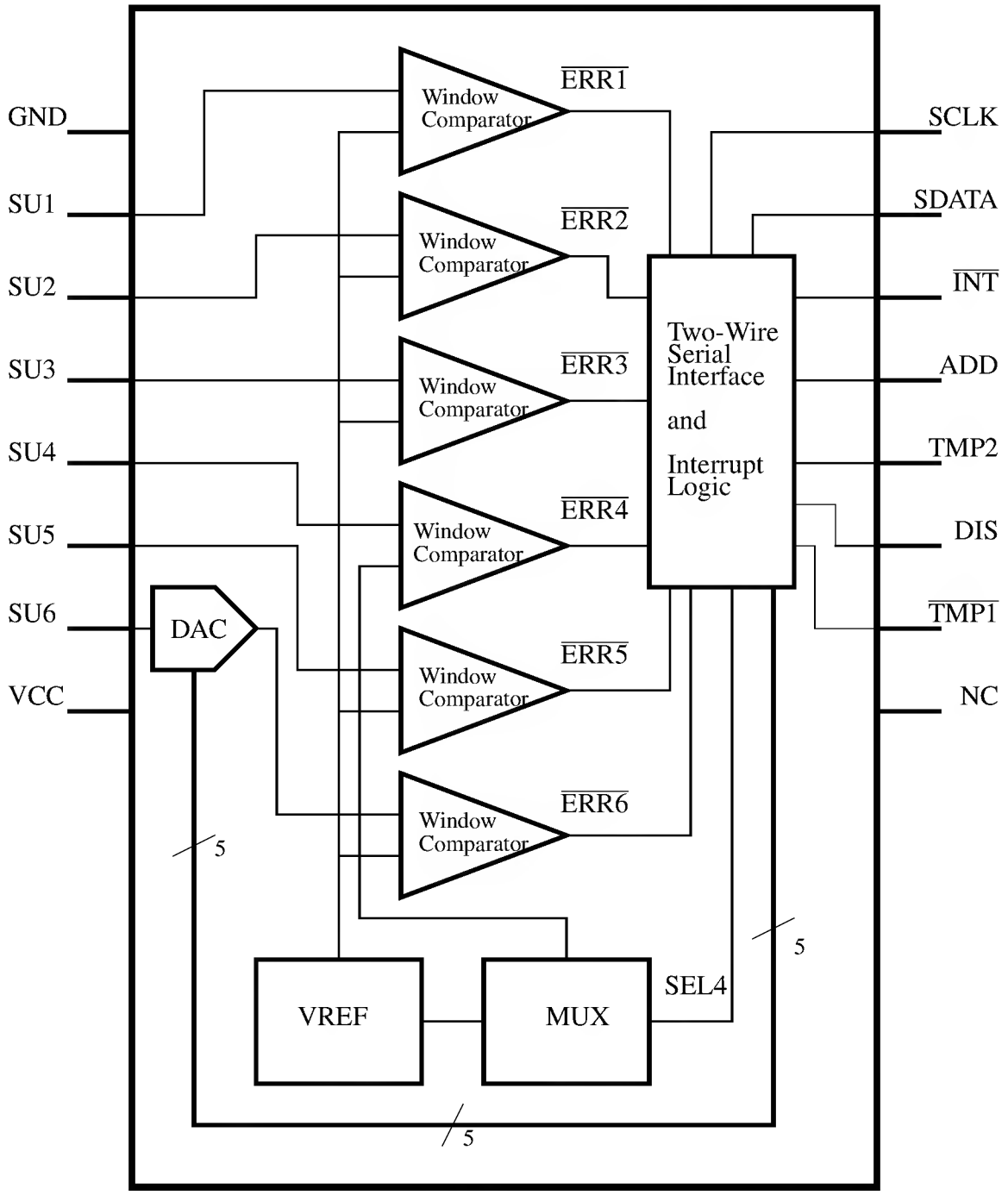
The SU6 input is normally used to monitor the CPU Core Voltage. The ADM9268 supports the range of CPU Core Voltage options from 1.3V to 3.5V which can be set up by a 5 bit VID code through the serial interface. This makes the ADM9268 compatible with all the CPUs currently available in the marketplace.

Analog Devices experience in the design of Power Supply Supervisory circuits is used to provide an optimum solution for the overall circuit in terms of cost, performance and power consumption. Some of the features of the design being the incorporation of hysteresis and glitch immunity into the comparators.

The part will be manufactured on one of Analog Devices' proprietary BiCMOS processes which also includes high performance thin film resistors to achieve the accuracy required for the precision voltage reference and power supply high and low trip points.

Hardware Monitor with Serial Interface

16 Pin Narrow SOIC Package



Pin Description

Pin Name	Pin No	Function
GND	1	Ground.
SU1	2	Supply to be monitored. 12V +/- 6%.
SU2	3	Supply to be monitored. 5V +/- 7%.
SU3	4	Supply to be monitored. 3.3V +/- 7%.
SU4	5	Supply to be monitored. 2.5V or 3.3V +/- 7%. Selected by SEL4.
SU5	6	Supply to be monitored. 1.5V +/- 7%.
SU6	7	Supply to be monitored. CPU Core Voltage +/- 5%.
VCC	8	Supply Monitor IC Power Supply. Can be powered off any Power Supply between 2.5V and 6V.
NC	9	No Connect.
$\overline{\text{TMP1}}$	10	TTL I/P. Event Input from Temperature Sensor - Active Low
DIS	11	TTL I/P. Disables ADM9268 when High, ie $\overline{\text{INT}}$ is forced High.
TMP2	12	TTL I/P. Event Input from Temperature Sensor - Active High.
ADD	13	TTL I/P. LSB of Address of Two-Wire Serial Interface.
$\overline{\text{INT}}$	14	Open Drain Output. When DIS is High ADM9268 is disabled and $\overline{\text{INT}}$ pulls high through an external 10k resitor to a positive power supply. When DIS is Low $\overline{\text{INT}}$ acts as active Low Interrupt Output which can be fed to the corresponding input of the microcontroller. An interrupt is generated when any of the supply inputs goes in or out of tolerance or there is a change on $\overline{\text{TMP1}}$ or $\overline{\text{TMP2}}$. The interrupt is cleared when the interface is read at the acknowledge bit after the rising edge of the SCLK signal.
SDATA	15	Two-Wire Serial Interface Data I/O.
SCLK	26	Two-Wire Serial Interface Clock Input.

Preliminary Specifications

Parameter	Min	Typ	Max	Units	Comments
Operating Temp Range	-40		85	Deg C	Industrial (A Version)
VCC Supply Voltage	2.5		6	V	Can be powered from SU2 or SU3.
VCC Supply Current		50	100	uA	Current from SU1-6 not included.
SU1 Input Resistance		240		kOhm	I_{IN} ~ 50uA when SU1=12V
SU2 Input Resistance		100		kOhm	I_{IN} ~ 50uA when SU2=5V
SU3 Input Resistance		66		kOhm	I_{IN} ~ 50uA when SU3=3.3V
SU4 Input Resistance		50		kOhm	I_{IN} ~ 50uA when SU4=2.5V
SU5 Input Resistance		30		kOhm	I_{IN} ~ 50uA when SU5=1.5V
SU6 Input Resistance		TBD		kOhm	I_{IN} ~ TBD
SU1 High Trip Point	12.72	12.96	13.20	V	Measured with SU1 rising
SU2 High Trip Point	5.35	5.45	5.55	V	Measured with SU2 rising
SU3/4 High Trip Point	3.53	3.60	3.66	V	Measured with SU3/4 rising
SU4 High Trip Point	2.675	2.725	2.775	V	Measured with SU4 rising
SU5 High Trip Point	1.605	1.635	1.665	V	Measured with SU5 rising
SU6 High Trip Point	TBD	TBD	TBD	V	Measured with SU6 rising
SU1 Low Trip Point	10.80	11.04	11.28	V	Measured with SU1 falling
SU2 Low Trip Point	4.45	4.55	4.65	V	Measured with SU2 falling
SU3/4 Low Trip Point	2.94	3.00	3.07	V	Measured with SU3/4 falling
SU4 Low Trip Point	2.225	2.275	2.325	V	Measured with SU4 falling
SU5 Low Trip Point	1.335	1.365	1.395	V	Measured with SU5 falling
SU6 Low Trip Point	TBD	TBD	TBD	V	Measured with SU6 falling
SU1 Hysteresis		2		%	Measured at SU1 Pin
SU2 Hysteresis		2		%	Measured at SU2 Pin
SU3 Hysteresis		2		%	Measured at SU3 Pin
SU4 Hysteresis		2		%	Measured at SU4 Pin
SU5 Hysteresis		2		%	Measured at SU5 Pin
SU6 Hysteresis		2		%	Measured at SU6 Pin
Glitch Immunity		20		us	~100mV glitch on VCC or SU1-6
Propogation Delay		20		us	Delay from Supply going outside tolerance until output changes
TTL Input Low			0.8	V	4.0V < VCC < 4.0V
TTL Input High	2.4			V	4.0V < VCC < 6.0V
TTL Input Low			0.6	V	2.5V < VCC < 4.0V
TTL Input High	2.0			V	2.5V < VCC < 4.0V
Open Drain Output Low			0.4	V	10k External to Positive Supply V_+
Open Drain Output High	V_+ - 0.25			V	10k External to Positive Supply V_+
Supply Range for V+	2.5		6	V	V_+ can be different from VCC

Absolute Maximum Ratings

Input	Maximum Rating
VCC	-0.3V to +6V
SU1, SU2, SU3, SU4, SU5, SU6	-0.3V to +15V
All Other Inputs	-0.3V to VCC + 0.3V
All Outputs	-0.3V to +6V
Output Current $\overline{\text{INT}}$, SDATA	20mA

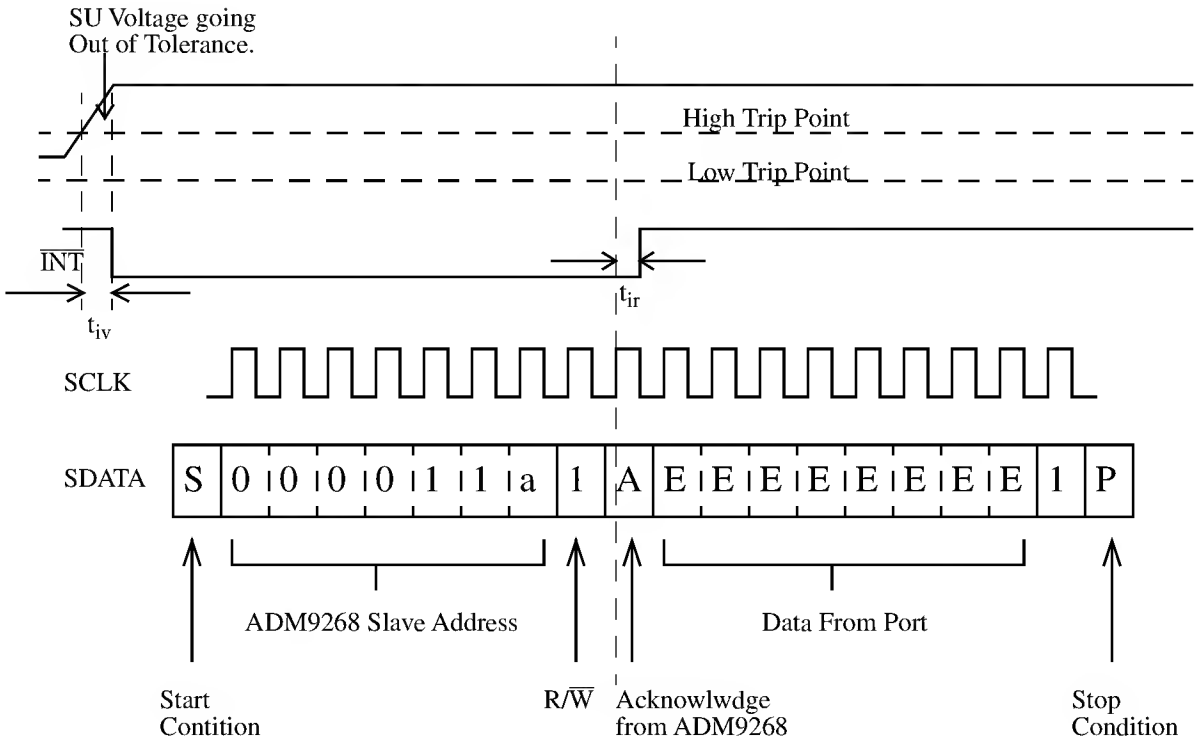
Selection of CPU Core Voltage

VID4	VID3	VID2	VID1	VID0	Voltage Monitored at SU6 Input
0	1	1	1	1	1.30V
0	1	1	1	0	1.35V
0	1	1	0	1	1.40V
0	1	1	0	0	1.45V
0	1	0	1	1	1.50V
0	1	0	1	0	1.55V
0	1	0	0	1	1.60V
0	1	0	0	0	1.65V
0	0	1	1	1	1.70V
0	0	1	1	0	1.75V
0	0	1	0	1	1.80V
0	0	1	0	0	1.85V
0	0	0	1	1	1.90V
0	0	0	1	0	1.95V
0	0	0	0	1	2.00V
0	0	0	0	0	2.05V
1	1	1	1	1	No CPU
1	1	1	1	0	2.1V
1	1	1	0	1	2.2V
1	1	1	0	0	2.3V
1	1	0	1	1	2.4V
1	1	0	1	0	2.5V
1	1	0	0	1	2.6V
1	1	0	0	0	2.7V
1	0	1	1	1	2.8V
1	0	1	1	0	2.9V
1	0	1	0	1	3.0V
1	0	1	0	0	3.1V
1	0	0	1	1	3.2V
1	0	0	1	0	3.3V
1	0	0	0	1	3.4V
1	0	0	0	0	3.5V

Operation of Two-Wire Serial Interface in Read Mode

When DIS is High the two-wire serial interface operates as an I^2C Compatible Interface.
The address of the port is 000011a where "a" is the logic level input to the ADD pin.
The ADM9268 operates as a slave device and whenever one of it's SU inputs goes in or out of tolerance or the $\overline{TMP1}$ or TMP2 inputs change state the $\overline{INT}$ pin goes low to indicate that there is new data available. $\overline{INT}$ goes high again at the acknowledge bit after the rising edge of the SCLK signal.

Figure 1: The following diagram shows the sequence of events.



The sequence of the bits in the Data Byte read from the ADM9268 Serial Port is as follows:

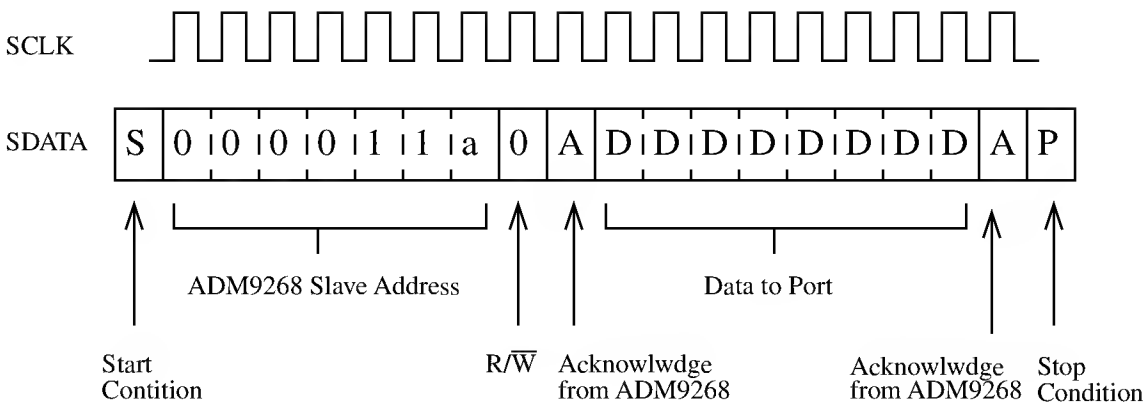
E7 - MSB (Read First)	$\overline{ERR1}$ (1 : in tolerance, 0 : out of tolerance)
E6	$\overline{ERR2}$ (1 : in tolerance, 0 : out of tolerance)
E5	$\overline{ERR5}$ (1 : in tolerance, 0 : out of tolerance)
E4	$\overline{ERR3}$ (1 : in tolerance, 0 : out of tolerance)
E3	$\overline{ERR6}$ (1 : in tolerance, 0 : out of tolerance)
E2	$\overline{ERR4}$ (1 : in tolerance, 0 : out of tolerance)
E1	$\overline{TMP1}$ (same logic level at $\overline{TMP1}$ input)
E0 - LSB (Read Last)	TMP2 (same logic level at TMP2 input)

Operation of Two-Wire Serial Interface in Write Mode

When DIS is High the two-wire serial interface operates as an I^2C Compatible Interface.
The address of the port is 000011a where "a" is the logic level on ADD input pin.

Write mode provides the ability to disable SU4 and SU5 in cases where these supplies are not in fact present and to also select which supply voltage is monitored on SU4. The CPU Core voltage monitored on SU6 can also be set through the Serial Interface.

A feature to note on this mode is that on Power-Up SU3 and SU4 are disabled and not enabled until valid data is written to the ADM9268 to select the correct settings for DIS4, DIS5 and SEL4. This guards against the possibility of SU4 or SU5 being flagged as being out of tolerance before the correct settings have been made. The VID bits also power up at 1 such that SU6 is disabled.



The sequence of the bits in the Data Byte written to the ADM9268 Serial Port is as follows:

VID4 (Written First)	CPU Core Voltage Selection Bit
VID3	CPU Core Voltage Selection Bit
VID2	CPU Core Voltage Selection Bit
VID1	CPU Core Voltage Selection Bit
VID0	CPU Core Voltage Selection Bit
DIS4	DIS4=1 disables SU4. DIS4=0 enables SU4.
DIS5	DIS5=1 disables SU5. DIS5=0 enables SU5.
SEL4 (Written last)	SEL4=1 means SU4 monitors 2.5V +/- 7%, SEL4=0 means SU4 monitors 3.3V +/- 7%.

Serial Bus Preliminary Specifications

Parameter	Min	Typ	Max	Units	Comments
V_{IL} (LOW Level I/P)	-0.3		+0.3xVCC	V	SCLK and SDATA Pins
V_{IH} (HIGH Level I/P)	0.7xVCC		VCC+0.3	V	SCLK and SDATA Pins
I_{OL} (LOW O/P Current)	3			mA	SDATA Pin
I_{IL} (I/P Lkg Current)			1	uA	SCLK and SDATA Pin
C_I (Input Capacitance)			7	pF	SCLK and SDATA Pins
I_{OL} (Low O/P Current)	1.6			mA	INTB Pin
I_{IL} (I/P Lkg Current)			1	uA	INTB Pin
t_{iv} (I/P Data Valid Time)			4	us	See Figure 1, CL <100pF
t_{ir} (Reset Delay Time)		15		us	See Figure 1, CL <100pF
f_{SCLK} (Clock Frequency)			100	kHz	See Figure 2
t_{SW} (Glitch Immunity)			100	ns	See Figure 2
t_{BUF} (Bus Free Time)	4.7			us	See Figure 2
$t_{SU;STA}$ (Start Setup)	4.7			us	See Figure 2
$t_{HD;STA}$ (Start Hold)	4.0			us	See Figure 2
t_{LOW} (SCLK Low Time))	4.7			us	See Figure 2
t_{HIGH} (SCLK High Time)	4.0			us	See Figure 2
t_r (SCLK, SDATA Rise)			1.0	us	See Figure 2
t_f (SCLK, SDATA Fall)			0.3	us	See Figure 2
$t_{SU;DAT}$ (Data Setup)	250			ns	See Figure 2
$t_{HD;DAT}$ (Data Hold)	0			ns	See Figure 2
$t_{VD;DAT}$ (Data Valid)			3.4	us	See Figure 2
$t_{SU;STO}$ (Stop Setup)	4.0			us	See Figure 2

Figure 2: Serial Bus Timing Diagram